CLAIMS

What is claimed is:

1. A reference current generator for a magnetic random access memory being provided to multiple-states memory cell, including 4-states memory cell and more-than-4-state memory cell for data reading, comprising:

a plurality of reference elements with more than two different resistance characteristics using a plurality of bit lines; the reference elements being the same as the magnetic tunnel junctions of the memory cell and bearing the same voltages as the magnetic tunnel junctions;

the voltage the same as the voltage of the memory cell being crossly connected to the reference elements so as to generate a plurality of current signals; and a peripheral IC circuit being used for dividing the plurality of current signals by 2 so as to obtain a plurality of midpoint current reference signals.

2. The reference current generator of claim 1 being provided to a 4-states memory cell for data reading, wherein the reference element has two different resistance characteristics, using three bit lines, and generates three current signals and three midpoint

current reference signals.

3. The reference current generator of claim 2, wherein the reference element is preset with four memory states, which are $R_{1max}//R_{2max}$, $R_{1max}//R_{2min}$, $R_{1min}//R_{2max}$, and $R_{1min}//R_{2min}$, and based on the memory states, it generates three current signals, which are $(I_{11}+I_{10})$, $(I_{10}+I_{01})$ and $(I_{01}+I_{00})$, and three midpoint current reference signals, which are $(I_{11}+I_{10})/2$, $(I_{10}+I_{01})/2$ and $(I_{01}+I_{00})/2$.

4. The reference current generator of claim 1, wherein more than two (N) reference current generators are connected in parallel so as to generate the more accurate reference current signals.

5. The reference current generator of claim 3, wherein more than two (N) reference current generators are connected in parallel so as to generate three current signals, which are N $(I_{11}+I_{10})$, N $(I_{10}+I_{01})$ and N $(I_{01}+I_{00})$, and the peripheral IC circuit divides the current signals by 2N so as to obtain three midpoint current reference signals, which are $(I_{11}+I_{10})/2$, $(I_{10}+I_{01})/2$ and $(I_{01}+I_{00})/2$.

6. The reference current generator of claim 1 being provided to M-states memory cell for data reading, and applying (M-1) bit lines, generating (M-1) current

signals and (M-1) midpoint current reference values.

7. A reference midpoint current generator for a magnetic random access memory being provided to 2-states memory cell for data reading, comprising:

more than one reference elements using one bit line; the reference element being the same as the magnetic tunnel junction of the memory cell and bearing the same voltage as the magnetic tunnel junction;

a voltage the same as the memory cell being crossly connected to the reference element so as to generate a current signal; a peripheral IC circuit being used for dividing the current signal by 2 so as to obtain a midpoint current reference signal.

8. The reference midpoint current generator of claim 7, wherein the reference element is preset with two memory states, R_{max} and R_{min}, and based on this, the current signal $(I_{max}+I_{min})$ and midpoint current reference value $(I_{max}+I_{min})/2$ are generated.

9. The reference midpoint current generator of claim 7, wherein more than two (N) reference current generators are connected in parallel so as to generate a more accurate reference midpoint current signal.

10. The reference midpoint current generator of claim 9, wherein the current signal $N(I_{max}+I_{min})$ is

generated, and divided by the peripheral IC circuit by 2N so as to obtain a midpoint current reference value $(I_{max}+I_{min})/2$.